WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a memory cell block that consists of L memory cells each for storing 1-bit digital value, where L is an integer equal to mth power of 2, and stores memory data expressing a combination of digital values stored in the individual memory cells in terms of an M-bit digital value, where M is a positive integer equal to or greater than two;

search lines on which 1-bit digital values are set to be matched with the digital values stored in the memory cells;

a search data setting section for setting search data expressing the combination of the L-bit digital values in terms of the M-bit digital value by setting the 1-bit digital values on the L search lines;

a match section for making a match/mismatch decision between the memory data and the search data by matching the digital value stored in the memory cells constituting the memory cell block with the digital value set on the search lines connected to the memory cells; and

an output section for outputting a decision result of said match section.

2. The semiconductor memory according to claim 1, wherein said memory cell block stores the memory data expressing the combination of the digital values stored in the individual memory cells in terms of 3^M M-bit digital values consisting of ternary values "0", "1" and "X (don't care)", and wherein

said search data setting section sets the search data expressing the combination of L-bit digital values in terms of M-bit digital values by charging only one of the L search lines

connected to the memory cells constituting said memory cell block.

3. The semiconductor memory according to claim 1, wherein said memory cell block is composed of two CAM cells, each of which stores data expressing a combination of digital values stored in a pair of memory cells in terms of ternary values "0", "1" and "X (don't care)", said memory cell block storing memory data expressing one of 3^2 combinations of the data stored in said CAM cells in terms of a 2-bit digital value; and

said search data setting section charges only one of the four search lines connected to the memory cells constituting said memory cell block to set the search data expressing one of the combinations of the 4-bit digital values in terms of four 2-bit digital values.

4. The semiconductor memory according to claim 1, wherein each of said memory cells is composed as a dynamic-type memory cell comprising:

a MOS transistor disposed at an intersection of a lattice formed by word lines and bit lines intersecting with each other; and

a data storage capacitor for storing 1-bit digital value.

5. The semiconductor memory according to claim 4, wherein

said output section includes a match line that is precharged every time said match section carries out matching, and outputs a charge state of the match line after the matching as a decision result of the match/mismatch between the memory data and search data;

said match section includes first MOS transistors that have their gate electrodes connected to nodes of the data storage capacitors, and open and close paths to the match line in response to charge states of the data storage capacitors, and that have gate insulating films with a thickness enabling charges on the match line to be leaked to the data storage capacitors via the gate electrodes, and second MOS transistors that have their gate electrodes connected to the search lines, and open and close paths to a ground in response to charge states of the search lines, said first MOS transistors and second MOS transistors connecting the match line to the ground when they close the paths; and

a charge processor for charging the match line for a time longer than a time said search data setting section takes to charge the search lines to compensate for charges in the data storage capacitors by using charges on the match line flowing through gate leakage of said first MOS transistors.